1

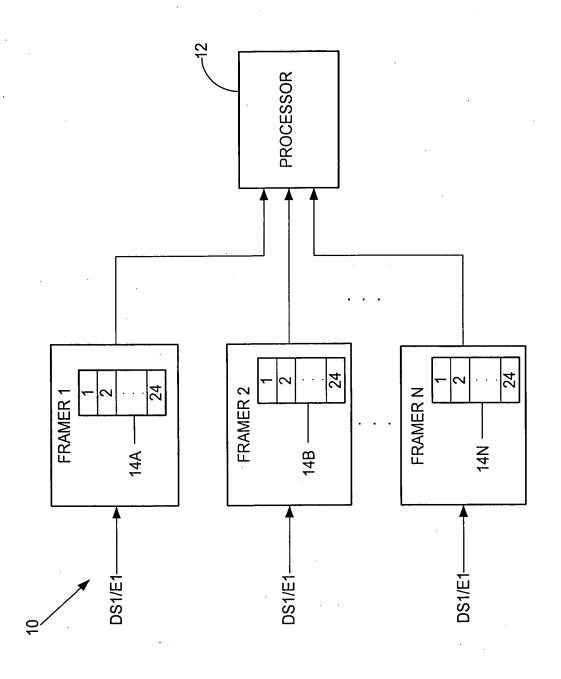
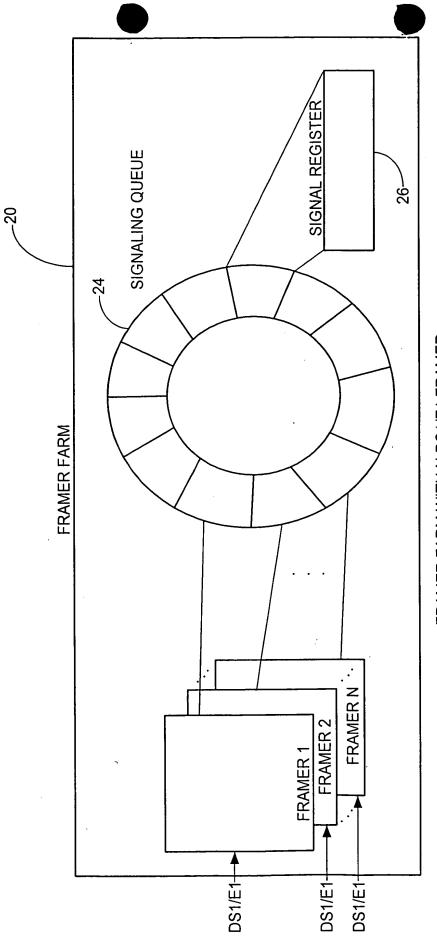


FIG. 1



FRAMER FARM WITH N DS1/E1 FRAMER

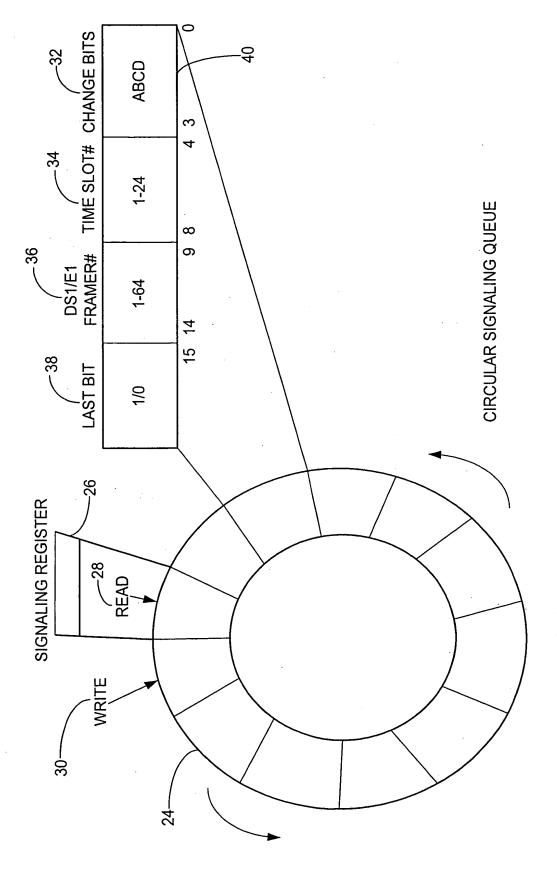


FIG. 3

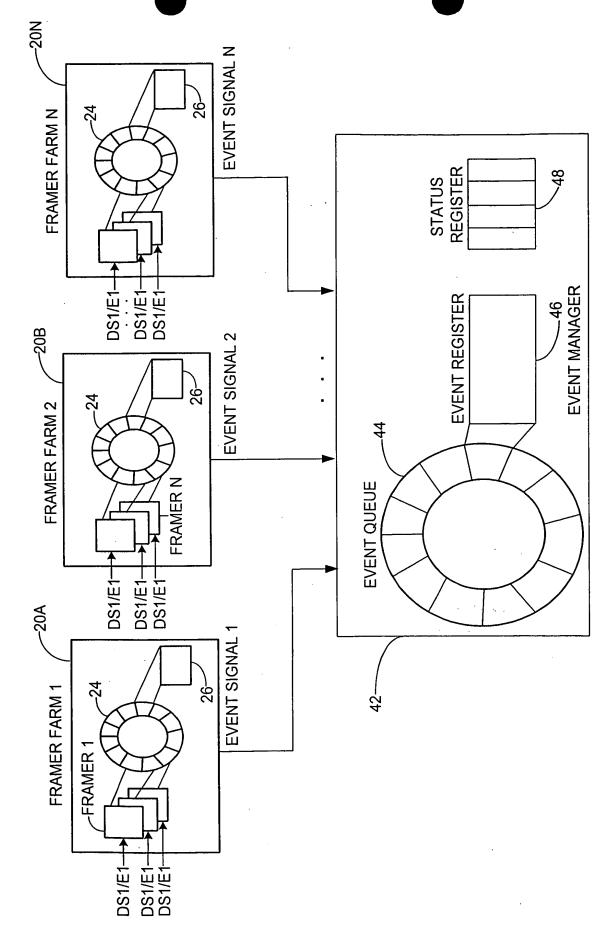


FIG. 4

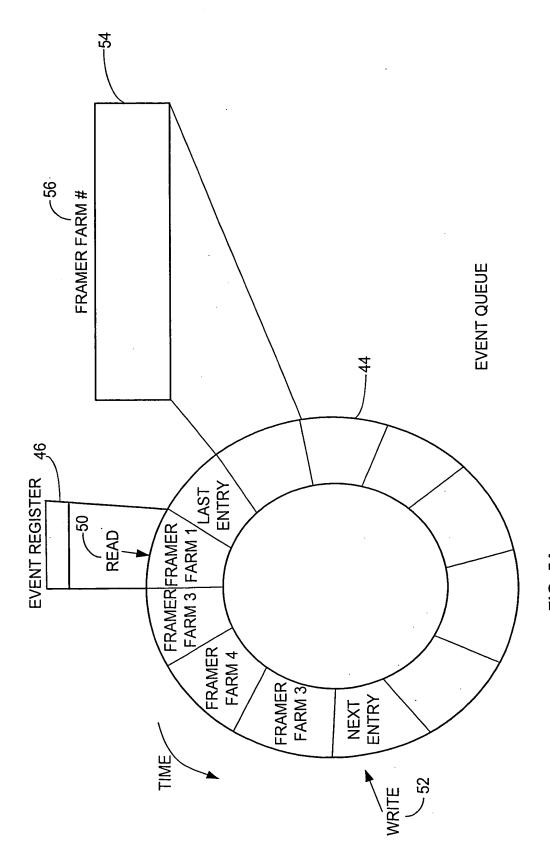


FIG. 5A

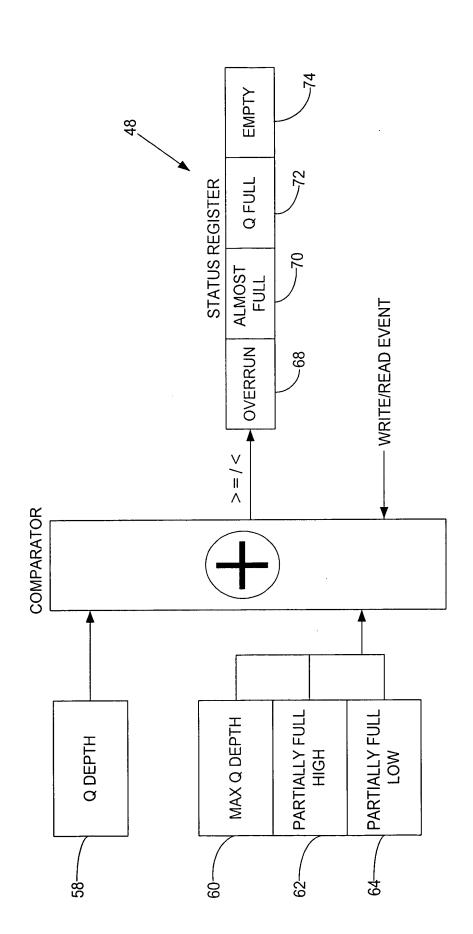


FIG. 5B

48 7 Ξ 10 က က 4 7 \sim 2/3/10,11 2. NEW ABCD CHANGE BITS

1/1/20,22

3. NEW ABCD CHANGE BITS

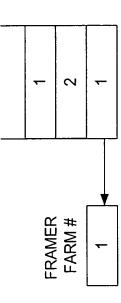
- 2 -

48

FIG. 6A

4. MICROPROCESSOR PROCESSES EVENTS

A. READS EVENT REGISTER



\	_		
	_	2	-

STATUS REGISTER

48

0

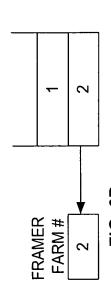
7		
		•

22	20	9	4
1	-	2	2
1	0	1	0
			4
			2

B. READS FRAMER FARM 1 SIGNALING REGISTER

	22	20	9
:	1	-	2
	-	0	0
			9
			2

C. READS FRAMER FARM 1 SIGNALING REGISTER



D. READS EVENT REGISTER

0

48

FIG. 6B

4. MICROPROCESSOR PROCESSES EVENTS

E. READS FRAMER FARM 2 SIGNALING REGISTER

0 3 10

F. READS FRAMER FARM 2 SIGNALING REGISTER

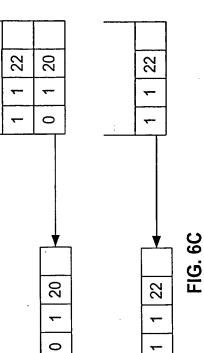
1 3 11

G. READS EVENT REGISTER



H. READS FRAMER FARM 1 SIGNALING REGISTER

I. READS FRAMER FARM 1 SIGNALING REGISTER



1/2/4

1/2/6

2/3/10

2/3/11

1/1/20

1/1/22

. . .

FRAMER FARM 1 SIGNALING QUEUE

FRAMER FARM 2 SIGNALING QUEUE

1

1	2	6	
0	2	4	

4

2

1	2	6	
0	2	4	

3

1	1	22	
0	1	20	
0	2	6	
0	2	4	

1 3 11 0 3 10

FIG. 8

PROCESSOR

1/2/4

1/2/6

1/1/20

1/1/22

2/3/10

2/3/11

FIG. 9